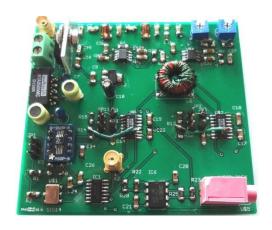


SDR_Ursinho

Design, Simulation and Assembly of a

Direct Conversion High Frequency

SDR Software Defined Receiver



Jeremy Clark VE3PKC



Copyright Information



© Clark Telecommunications/Jeremy Clark/August 2016

All rights reserved. No part of this work shall be reproduced, stored in a retrieval system or transmitted by any means, electronic, mechanical, photocopying, recording, or otherwise, without the written permission of the author. No patent liability is assumed with respect to the use of the information contained herein. Although every precaution has been taken in the preparation of this book, the author assumes no responsibility for errors, omissions, inaccuracies or any inconsistency herein. Nor is any liability assumed for damages resulting from the use of the information contained herein.

This work is sold as is, without any warranty of any kind, either express or implied, respecting the contents of this book, including but not limited to implied warranties for the book's quality, performance, merchantability, or fitness for any particular purpose.

Clark Telecommunications
Jeremy Clark
500 Duplex Suite 506
Toronto M4R-1V6, Ontario, Canada
416-488-5382
iclark@clarktelecommunications.com
www.clarktelecommunications.com

Table of Contents

1 - Introduction	1
1.1 - Design Philosophy1.2 - Block & Level Diagram1.3 - Development Environment1.4 - Hartley Direct Conversion Simulation	1 1 2 2
2 - BPF Band Pass Filter Design	5
2.1 - BPF ELSIE Design2.2 - BPF LTspice Simulation2.3 - BPF Hardware Measurement	5 7 8
3 - RF Amplifier Design	9
3.1 - AD603 Single Stage LTspice Simulation3.2 - AD603 Single Stage Hardware Measurement3.3 - AD603 Two Stage LTspice Simulation3.4 - AD603 Two Stage Hardware Measurement	9 10 11 13
4 - Mixer Design	14
4.1 - Mixer Simulation 4.2 - Mixer Hardware Measurement	14 15
5 - LPF Low Pass Filter Design	18
5.1 - LPF Low Pass Filter Simulation5.2 - LPF Low Pass Filter Corner Frequency LTC69045.3 - LPF Low Pass Filter Hardware Measurement	18 20 22
6 - VFO Variable Frequency Oscillator	25
6.1 - VFO Si514 6.2 - VFO Quad Circuit 6.3 - VFO Measurement	25 25 26
7 - Baseband Amplifier	28
7.1 - BB Amp OPA2134 Simulation 7.2 - BB Amp OPA2134 Measurement	28 29
8 - Power Supply Design	31
8.1 - Power Supply General 8.2 - Power Supply Measurements	31 31
9 - Schematic, PCB Design, Assembly and Testing	32
9.1 - SDR_UD Schematic Diagram 9.2 - PCB Printed Circuit Board Layout 9.3 - Block & Level Diagram Testing 9.4 - Assembly 9.4 1 - BPF Band Pass Filter	32 32 33 34

9.4.2 - PS Power Supply	35
9.4.3 - RF Amplifier	35
9.4.4 - Balun Balanced to Unbalanced Toroidal Transformer	36
9.4.5 - LPF Low Pass Filter Corner Frequency Clock LTC6904	36
9.4.6 - VFO Variable Frequency Oscillator Si514	37
9.4.7 - VFO Quad Circuit 74LS74D	37
9.4.8 - Mixer/LPF Low Pass Filter	38
9.4.9 - Baseband Amplifier OPA2134	38
10 - Baseband Signal Processing	39
10.1 - Windows 5KHz Base Band Signal Processing ScicosLab	39
10.2 - Windows 5KHz Base Band Signal Processing Spectravue & SDRADIO	41
10.3 - Windows 24KHz Base Band Signal Processing Spectravue & SDRADIO	42
10.4 - Linux 5KHz Base Band Signal Processing with GNU Radio Companion	43
11 - Conclusions	44
Appendix A - SDR_U Development Environment	45
Appendix B - I & Q Demodulation Math	48
Appendix C - Raspberry Pi Configuration	49
Appendix D - Python Documentation	5 1
Appendix E - LTC6904 Python Code	52
Appendix F - Si514 Python Code	53
Appendix G - Parts List	59
Glossary	60